

6042709-14493

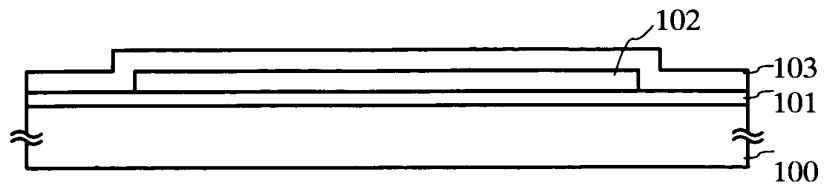


FIG. 1A

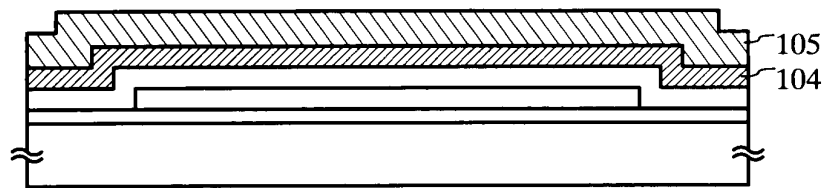


FIG. 1B

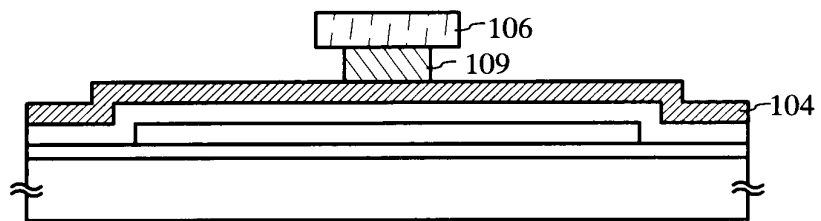


FIG. 1C

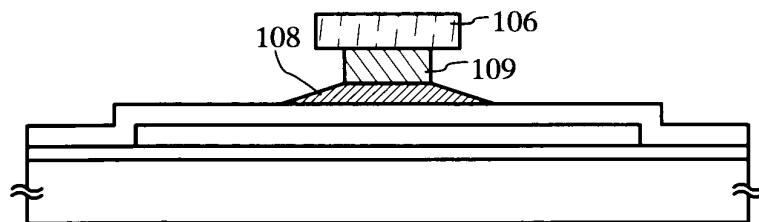


FIG. 1D

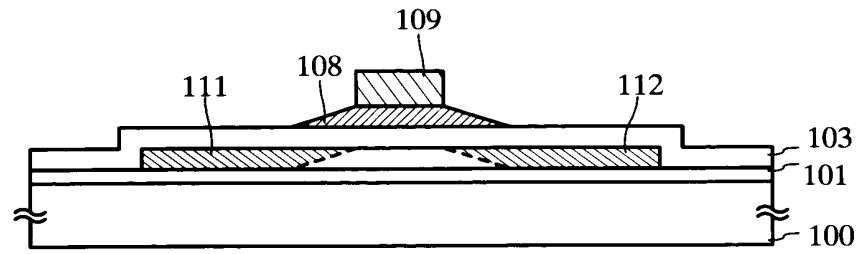


FIG. 2A

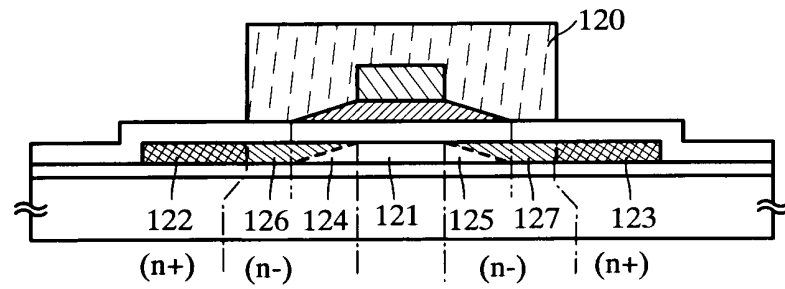


FIG. 2B

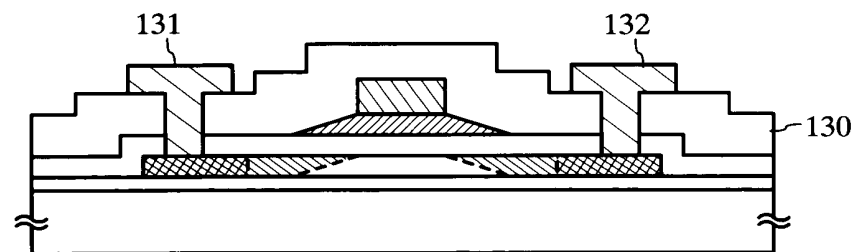


FIG. 2C

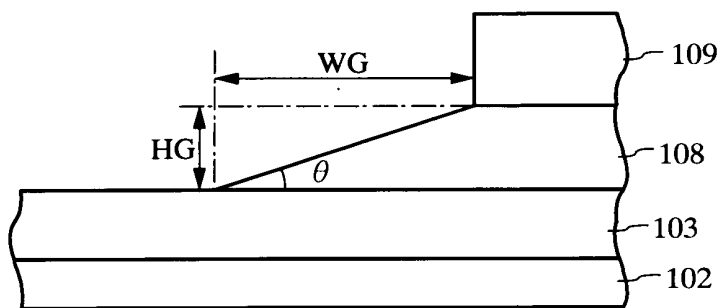
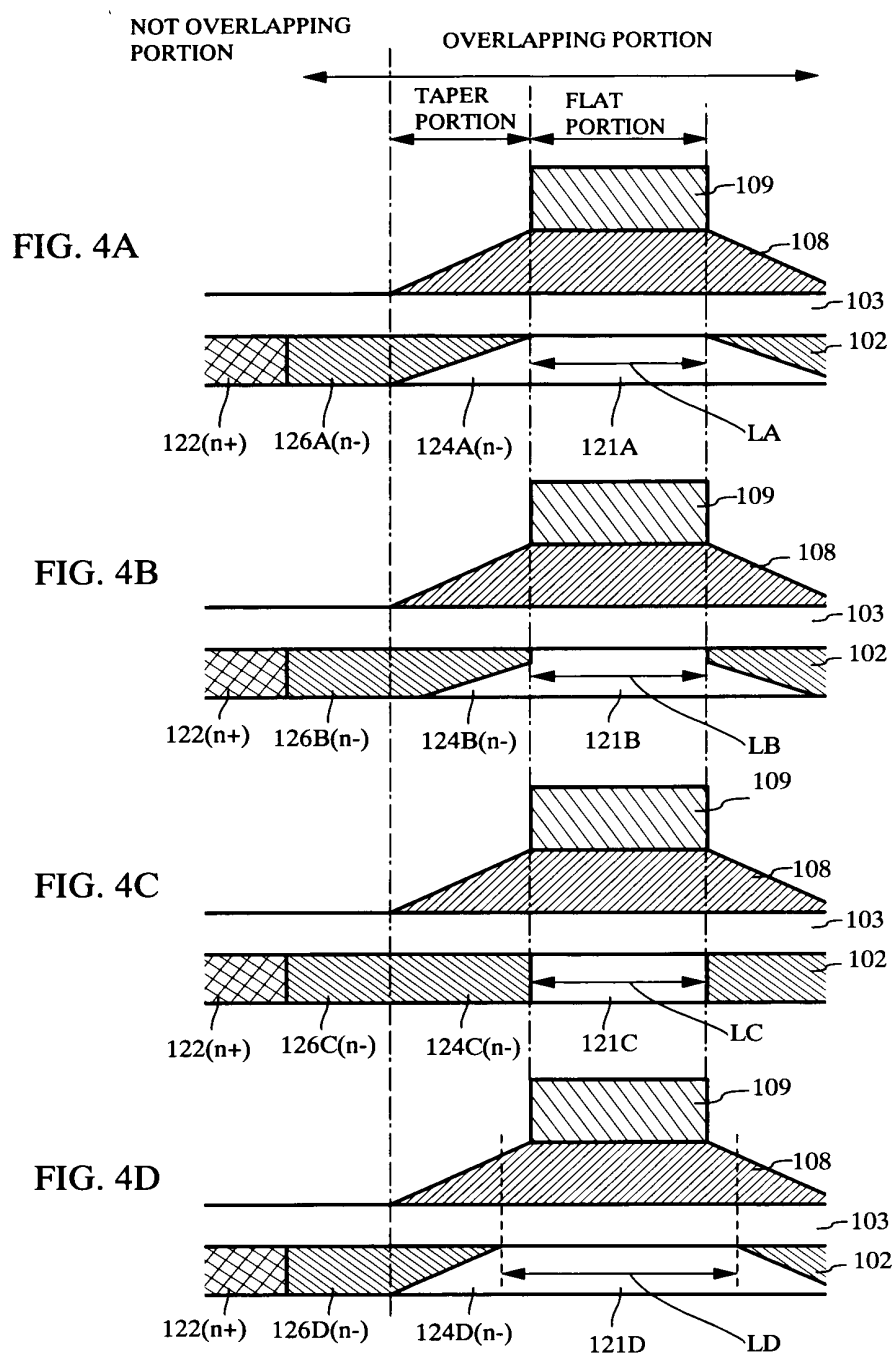


FIG. 3



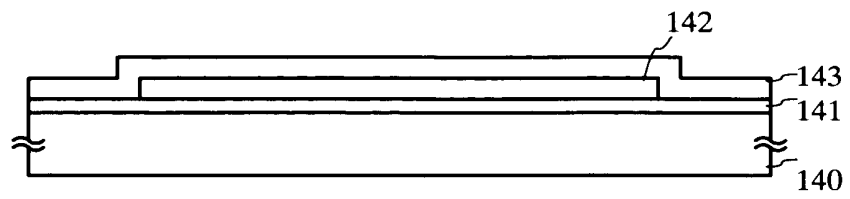


FIG. 5A

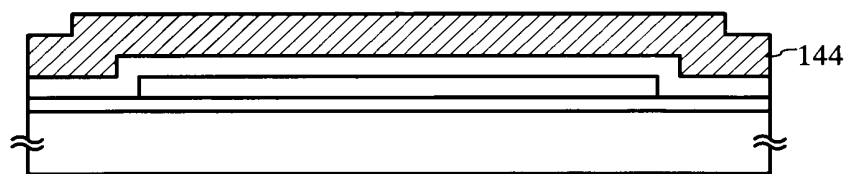


FIG. 5B

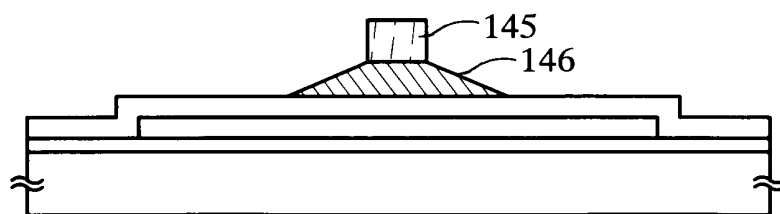


FIG. 5C

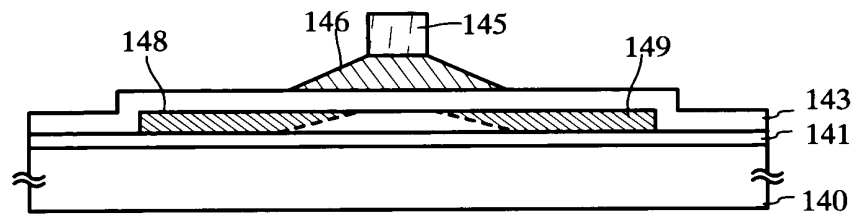


FIG. 6A

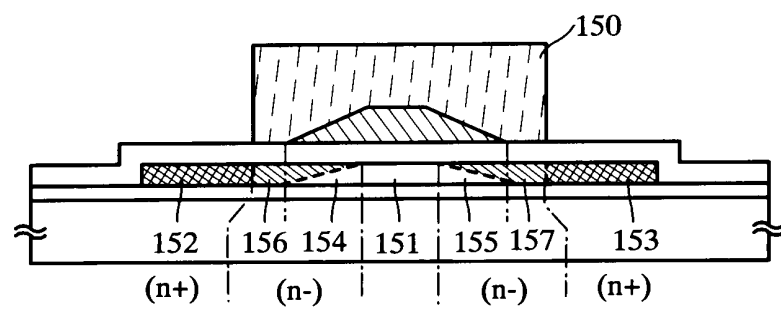


FIG. 6B

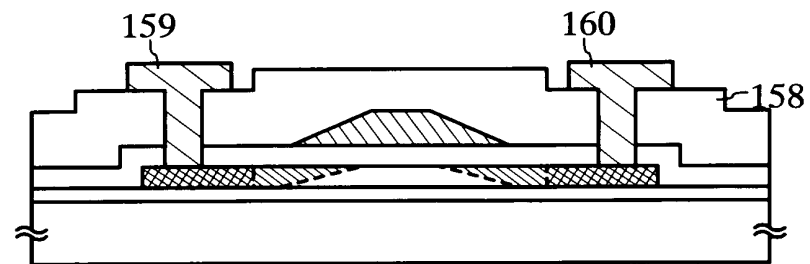


FIG. 6C

FIG. 7

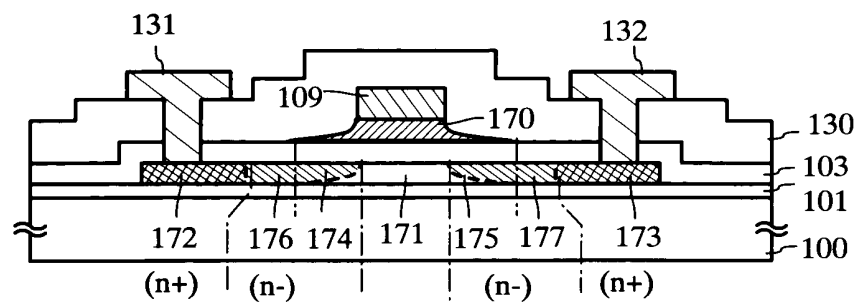


FIG. 8

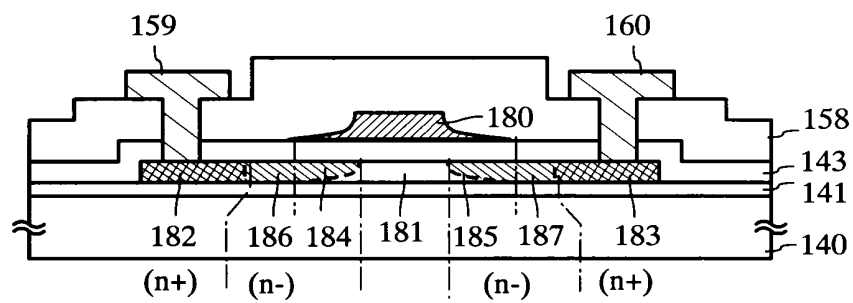


FIG. 9

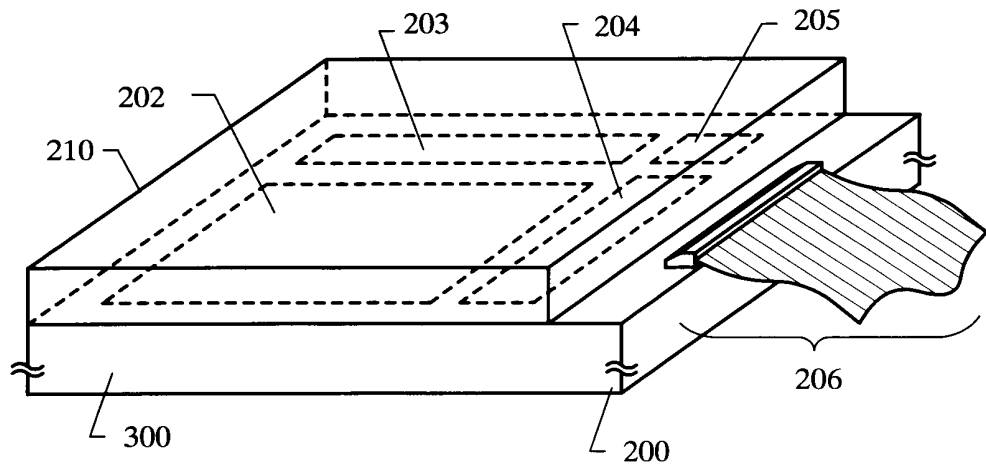


FIG. 10

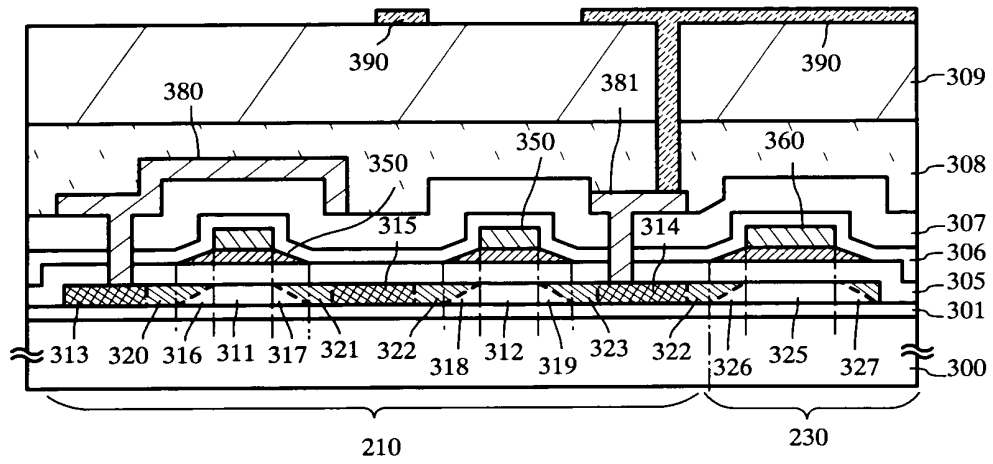


FIG. 12A

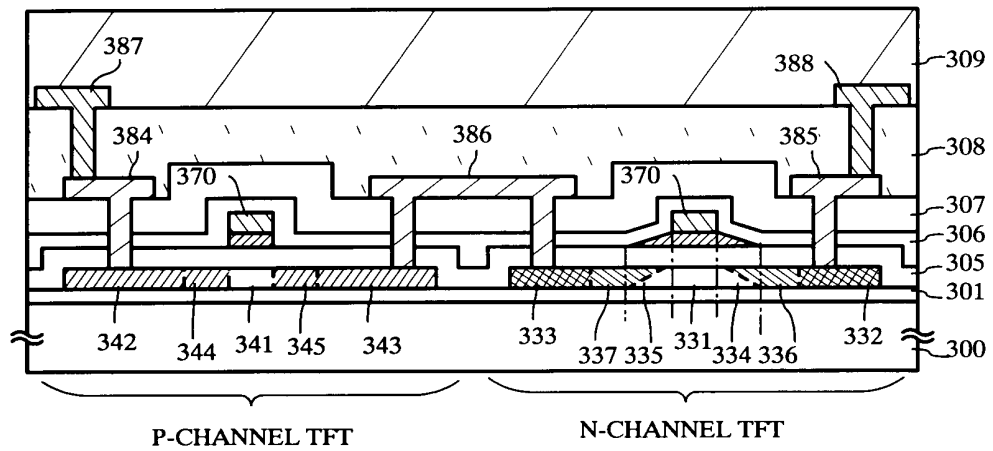


FIG. 12B

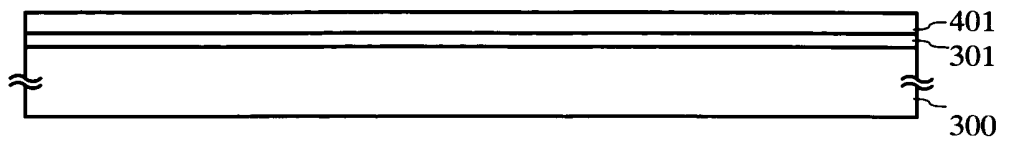


FIG. 13A

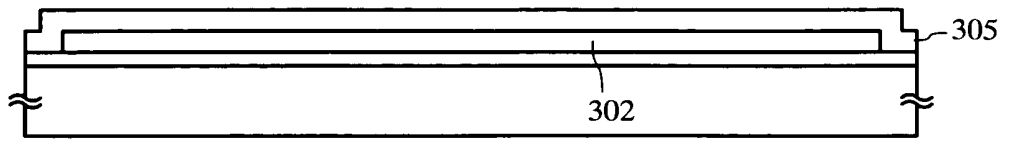


FIG. 13B

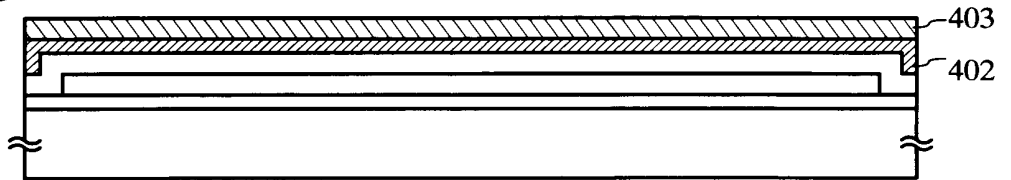


FIG. 13C

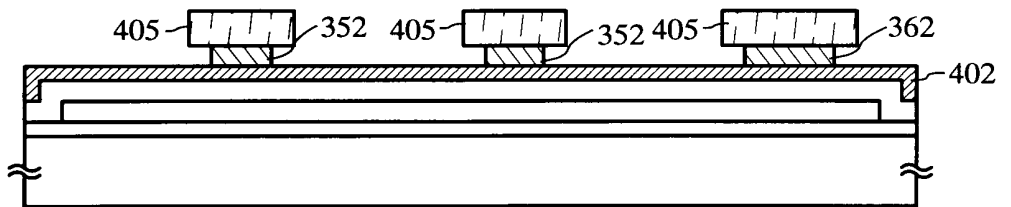


FIG. 13D

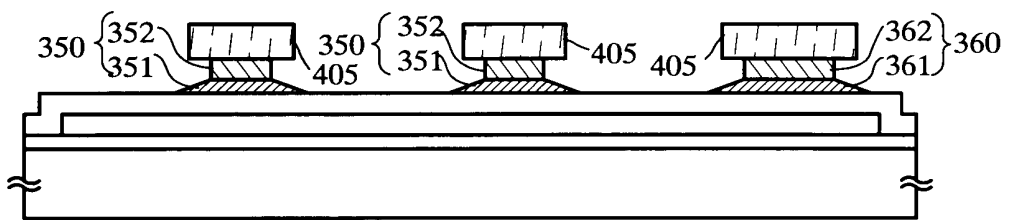


FIG. 13E

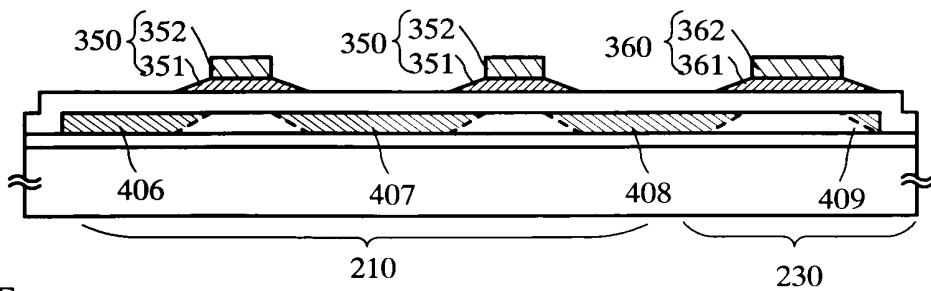


FIG. 13F

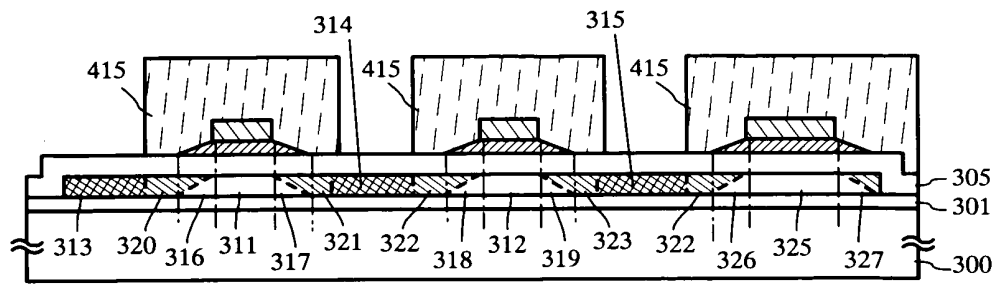


FIG. 14A

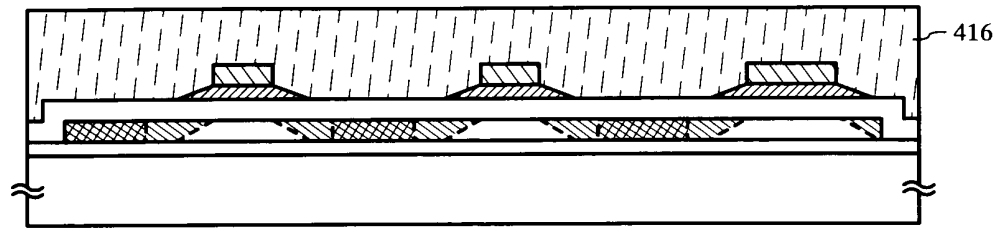


FIG. 14B

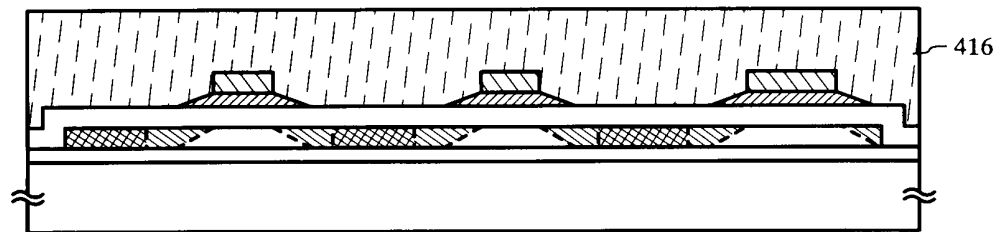


FIG. 14C

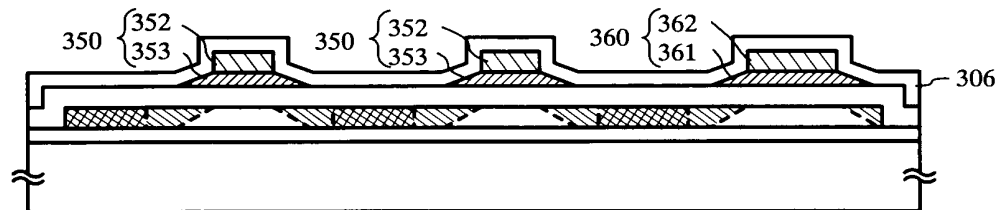


FIG. 14D

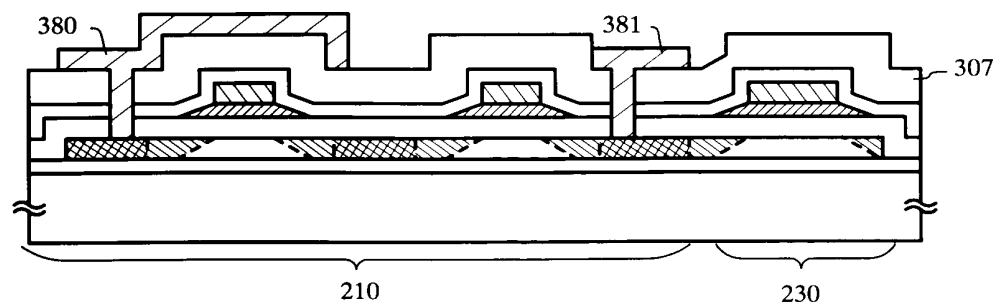


FIG. 14E

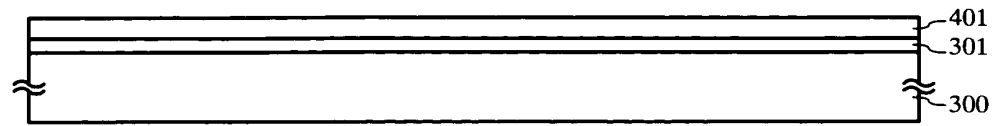


FIG. 15A

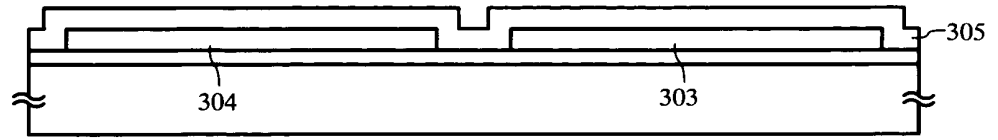


FIG. 15B

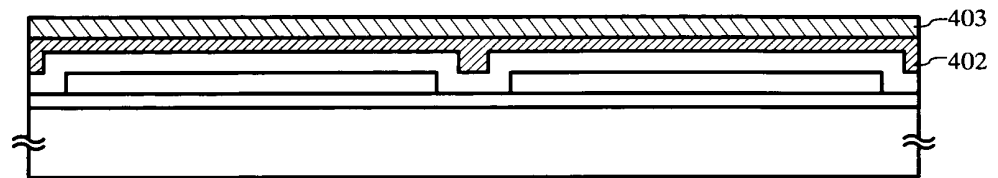


FIG. 15C

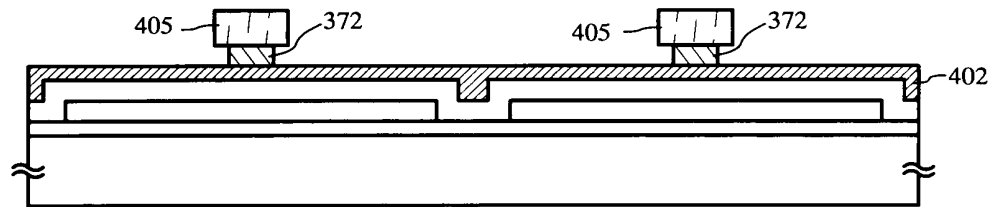


FIG. 15D

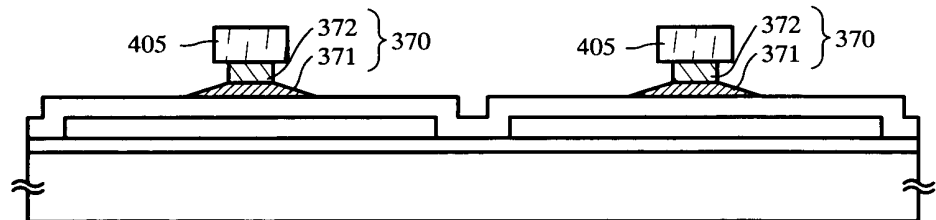


FIG. 15E

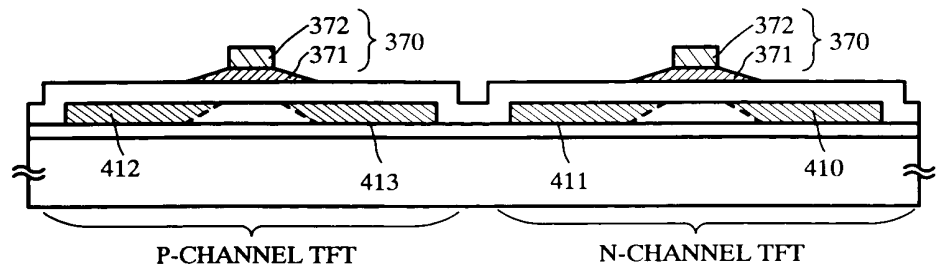


FIG. 15F

This diagram shows a cross-sectional view of a semiconductor device, similar to the first one but with an additional gate structure. A second gate electrode, labeled 370, is positioned on top of the first gate electrode 372. This second gate electrode is divided into two parts: 372' and 373'. The region 373' is located directly above the first gate electrode 372, while the region 372' is positioned above the channel region 371. The channel region 371 is the area between the two gate electrodes. The substrate 416 is shown at the bottom, with a p-type region 374 and an n-type region 375. The first gate electrode 372 is connected to a terminal 376, and the second gate electrode 370 is connected to a terminal 377. The device is shown with electrical connections at the bottom.

[illegible]

A cross-sectional view of a semiconductor device. It shows a substrate with a thin layer on top. A patterned layer with openings is on top of the thin layer. A top layer with a central opening is on top of the patterned layer. The top layer is labeled 306.

384 386 385 307

P-CHANNEL TFT N-CHANNEL TFT

FIG. 16E

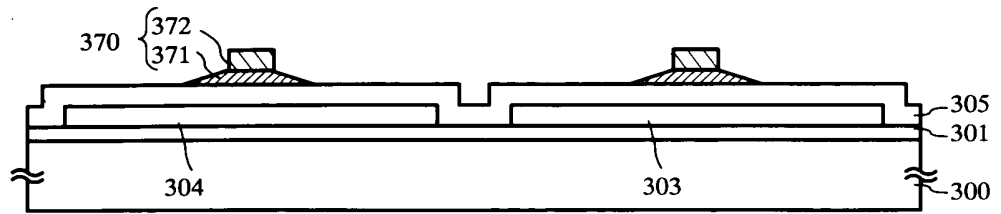


FIG. 17A

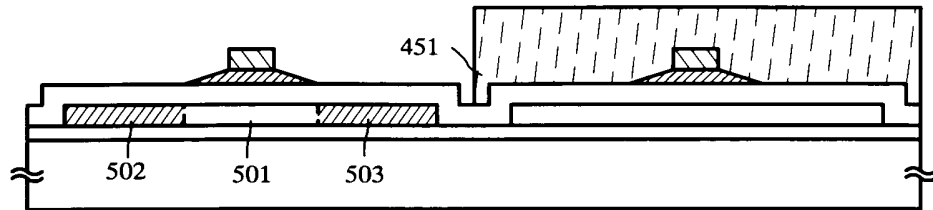


FIG. 17B

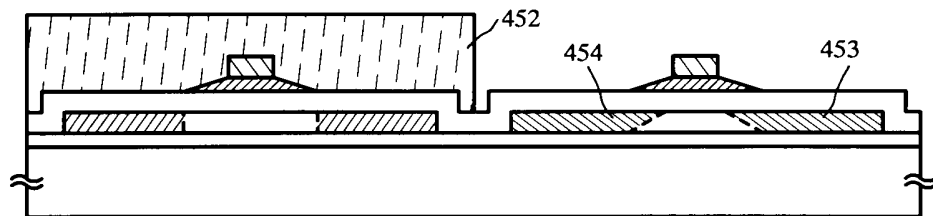


FIG. 17C

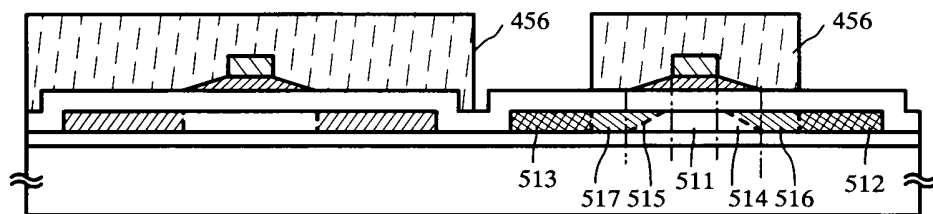


FIG. 17D

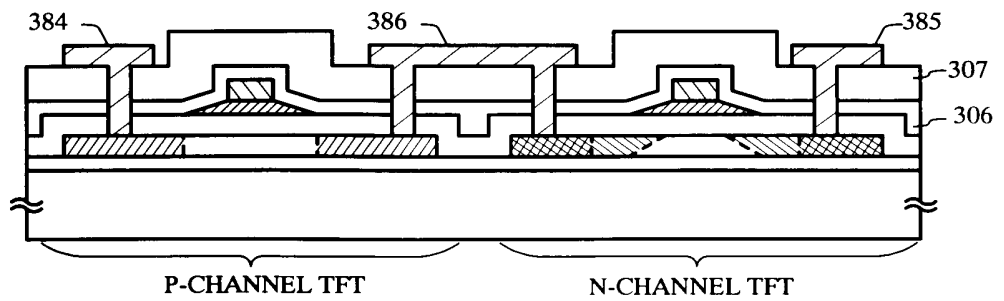


FIG. 17E

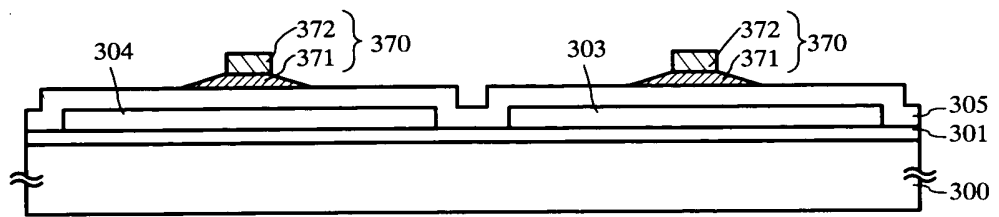


FIG. 18A

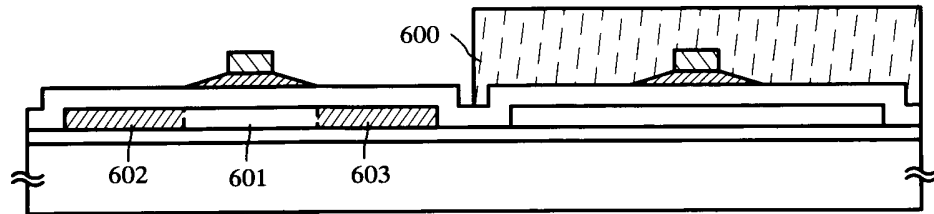


FIG. 18B

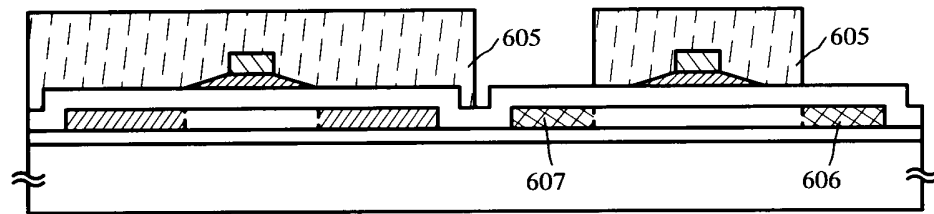


FIG. 18C

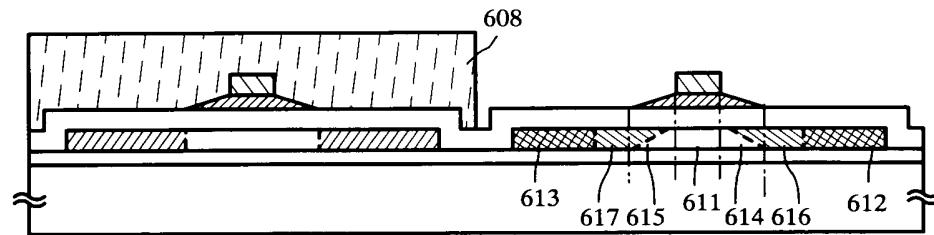


FIG. 18D

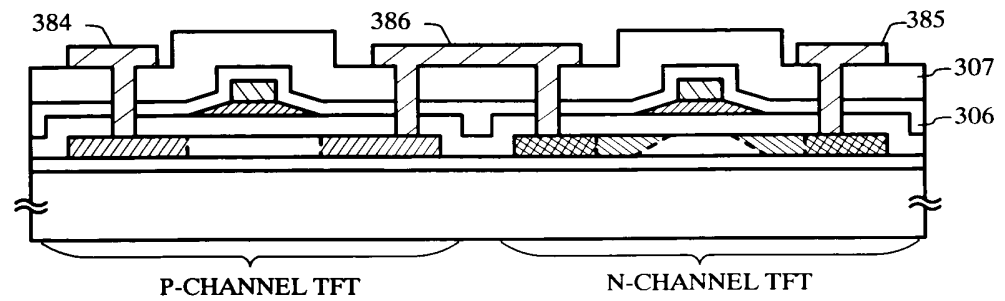
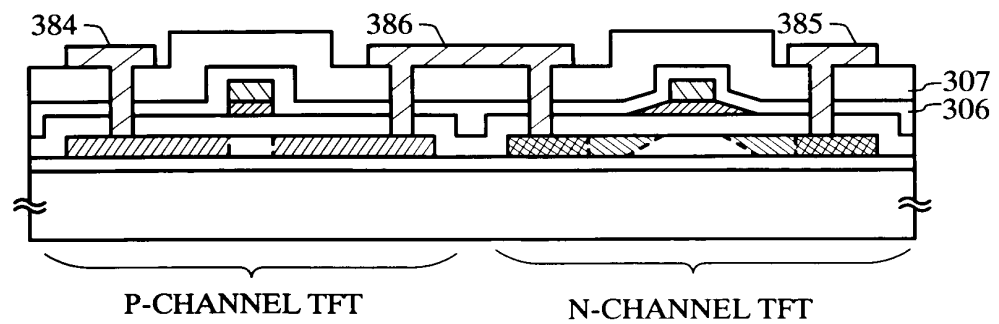


FIG. 18E



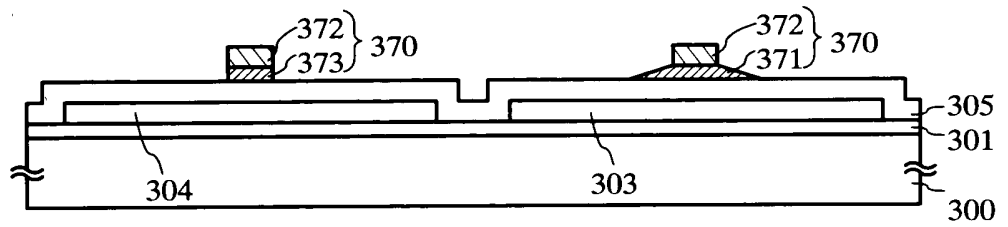


FIG. 21A

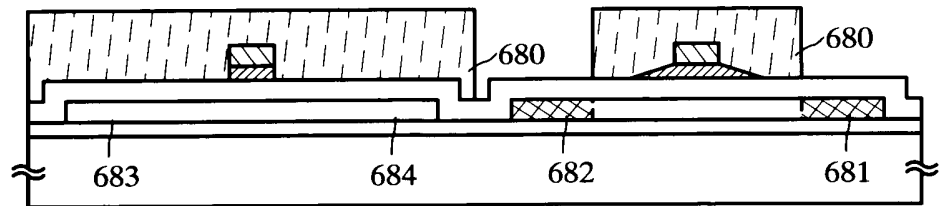


FIG. 21B

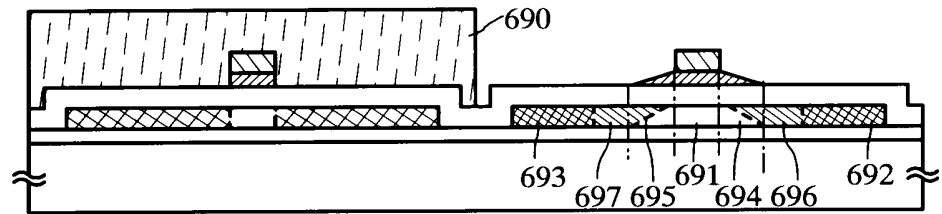


FIG. 21C

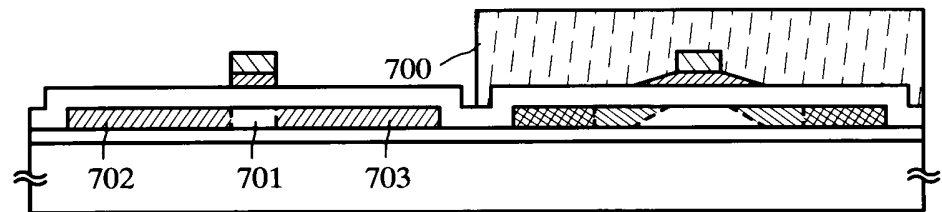


FIG. 21D

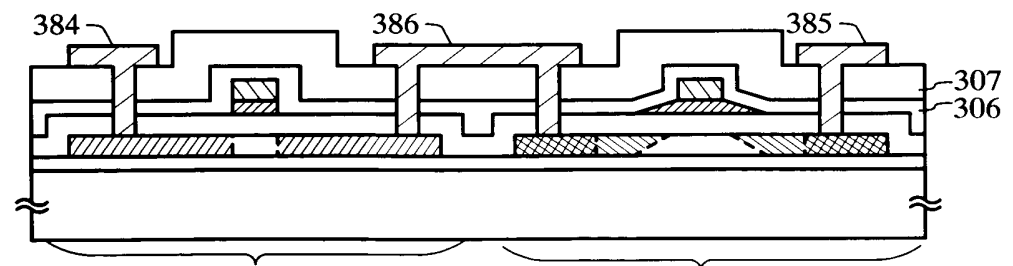


FIG. 21E

P-CHANNEL TFT

N-CHANNEL TFT

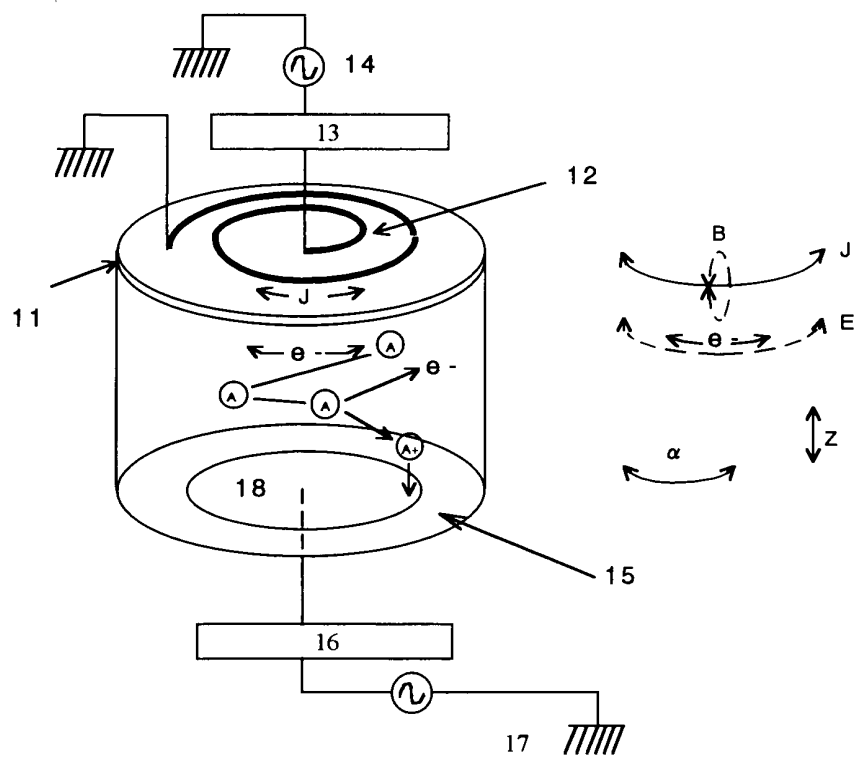


FIG. 22

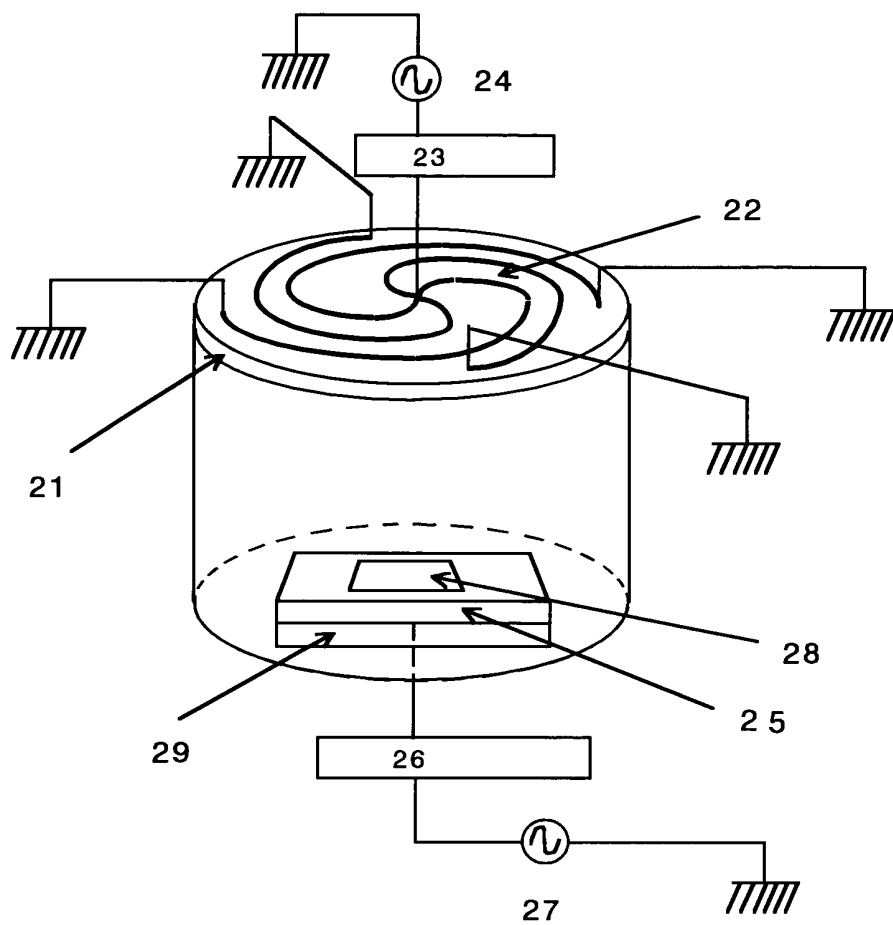


FIG. 23

ICP=500W Pressure=1.0Pa CF₄/Cl₂=30/30sccm

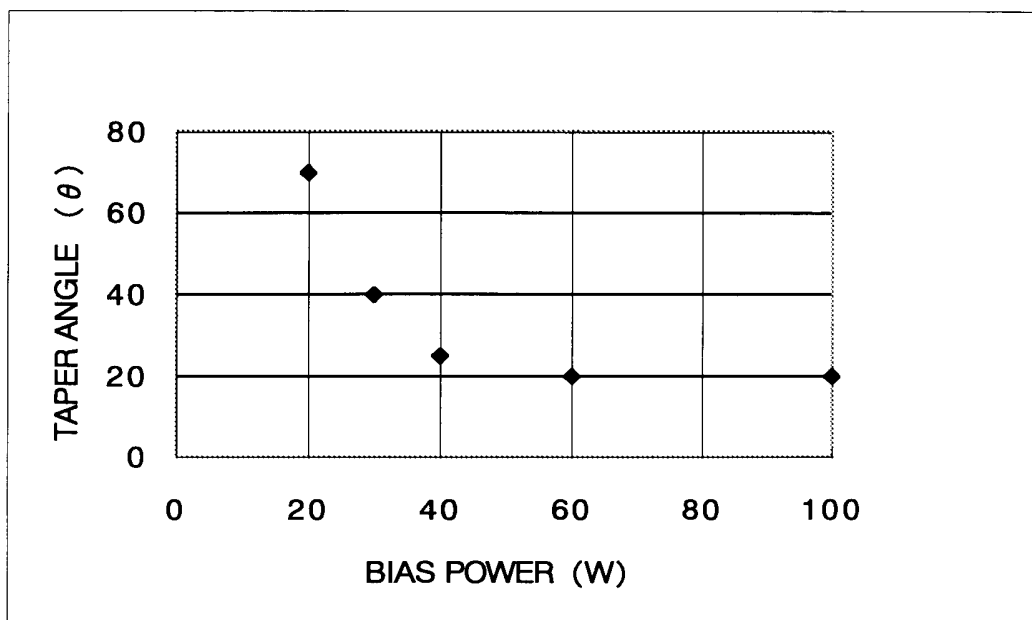


FIG. 24 DEPENDENCY OF TAPER ANGLE θ UPON BIAS POWER

ICP=500W Pressure=1.0PA $\text{CF}_4/\text{Cl}_2=30/30\text{sccm}$

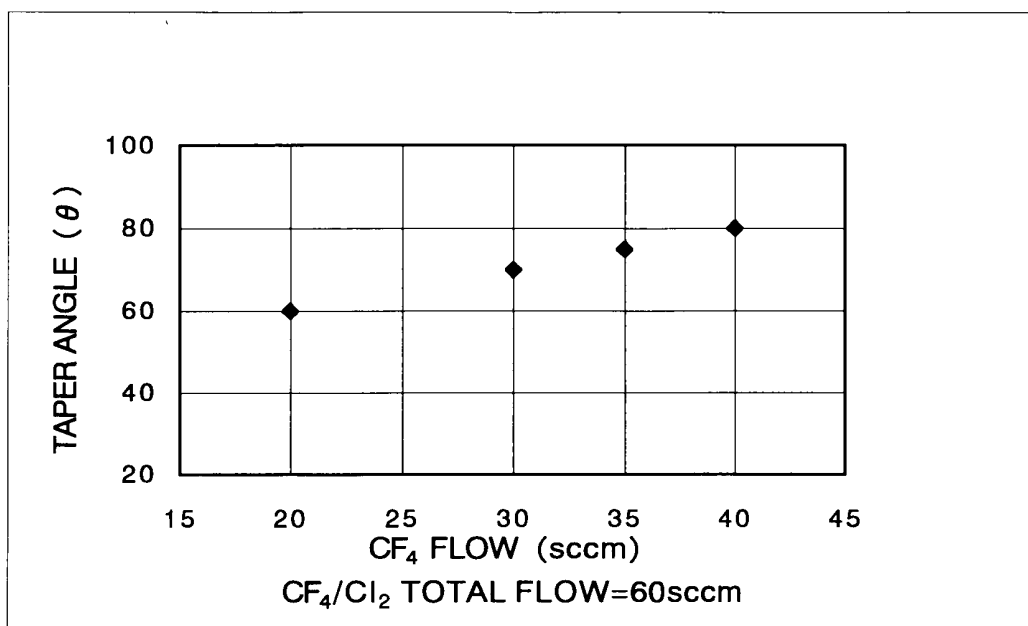


FIG. 25

DEPENDENCY OF TAPER ANGLE θ UPON CF_4 FLOW RATIO

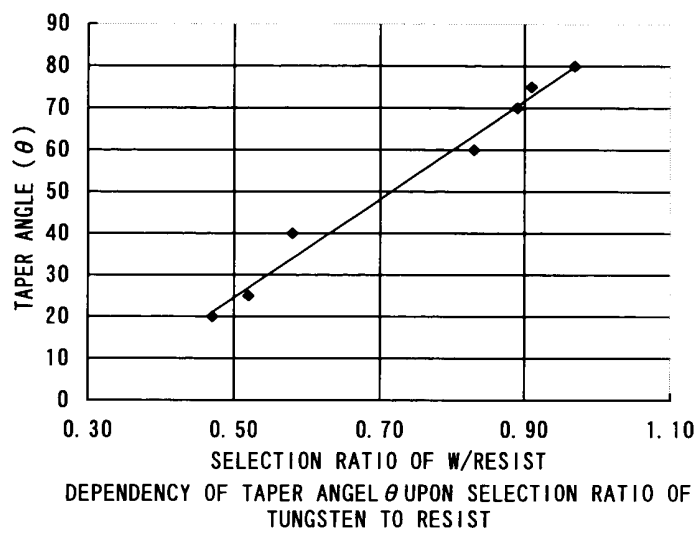


FIG. 26

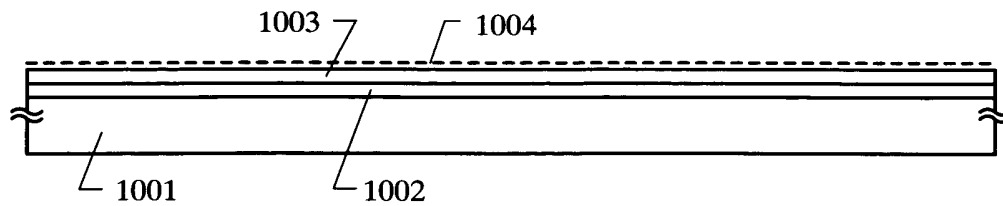


FIG. 27A

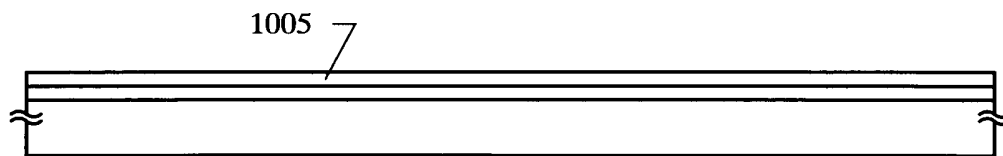


FIG. 27B

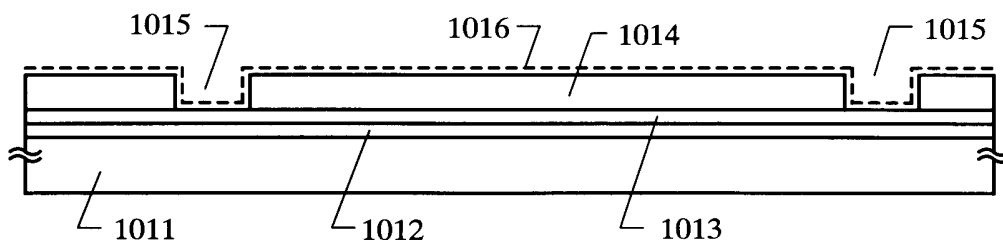


FIG. 28A

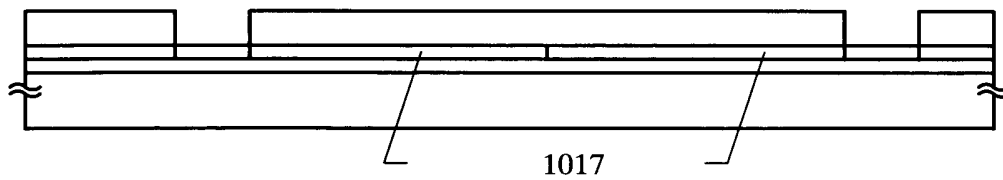


FIG. 28B

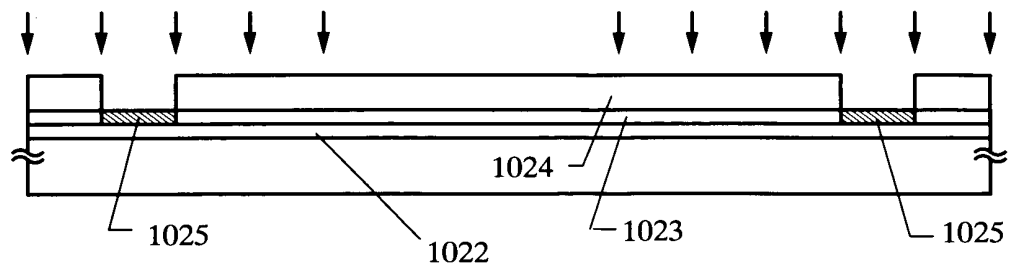


FIG. 29A

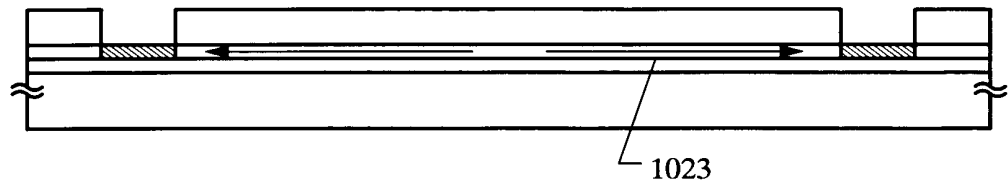


FIG. 29B

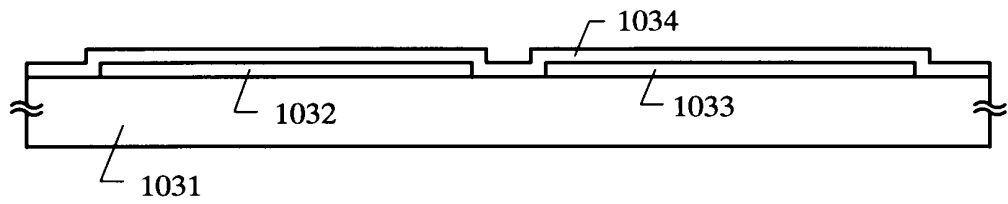
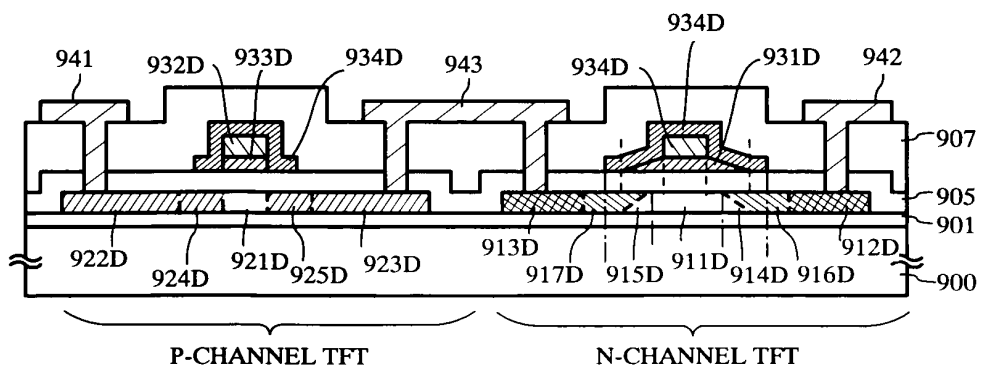


FIG. 30A



FIG. 30B



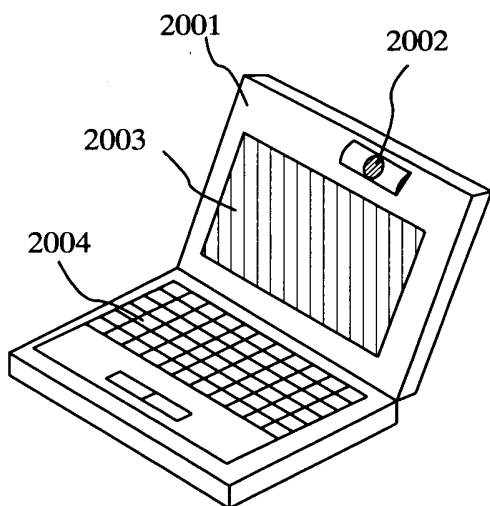


FIG. 32A

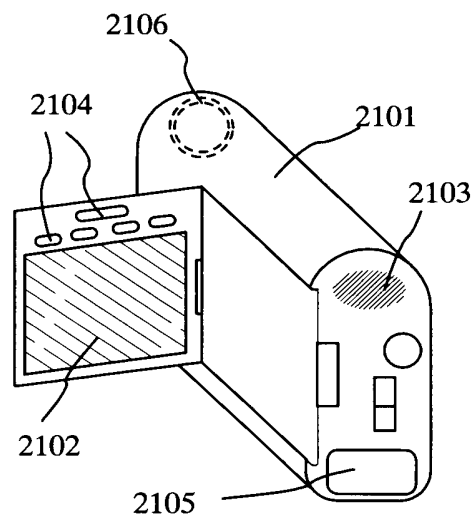


FIG. 32B

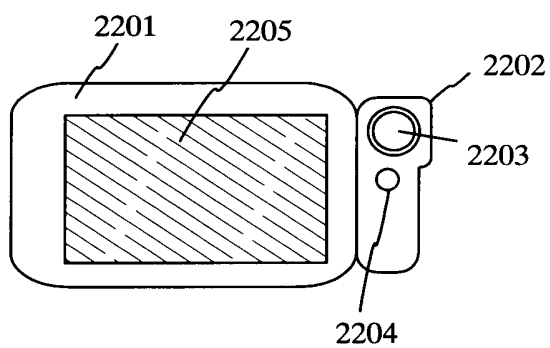


FIG. 32C

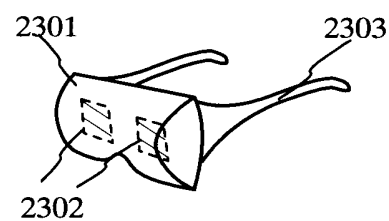


FIG. 32D

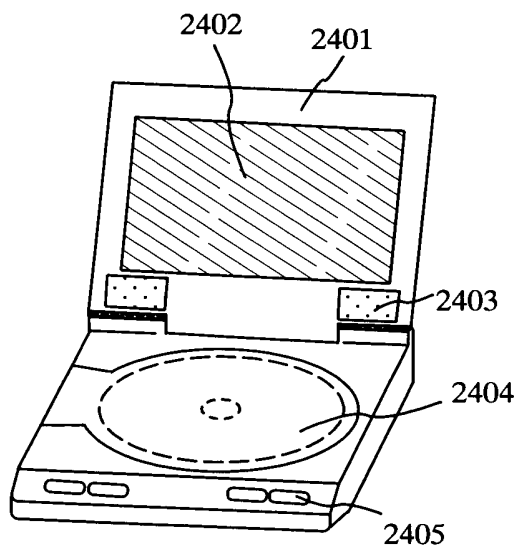


FIG. 32E

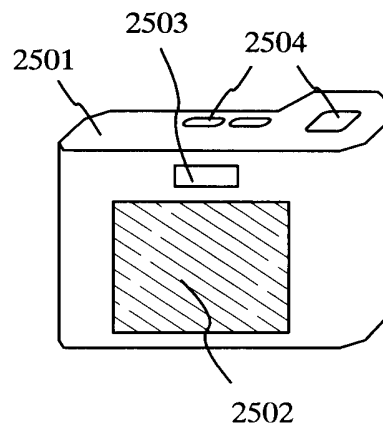


FIG. 32F

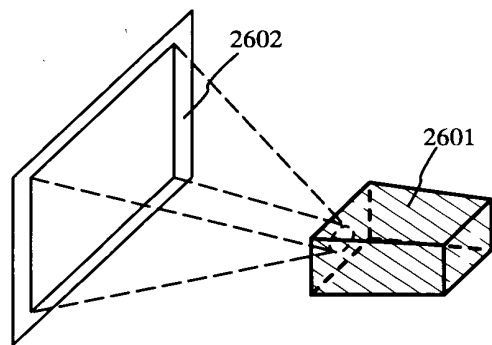


FIG. 33A

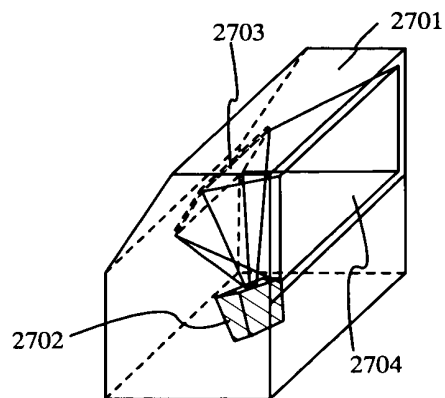


FIG. 33B

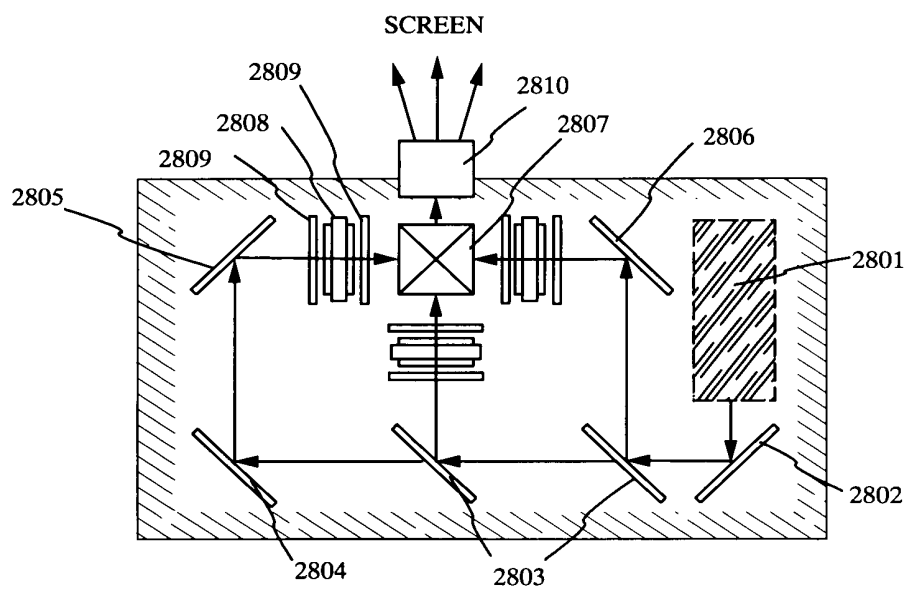


FIG. 33C

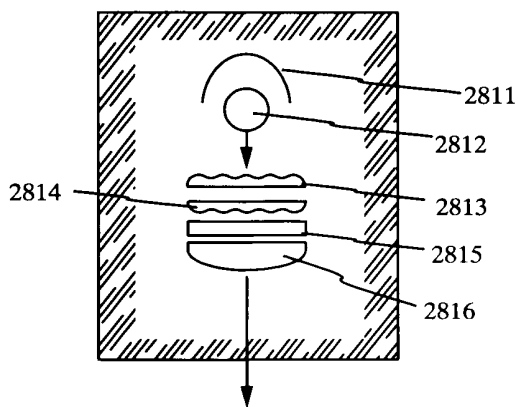


FIG. 33D

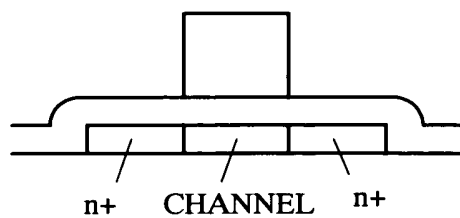


FIG. 34A

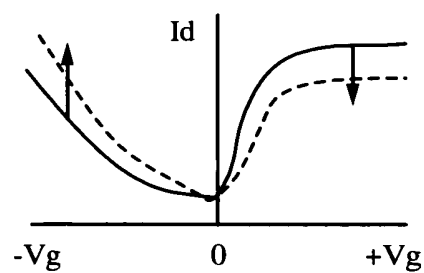


FIG. 34B

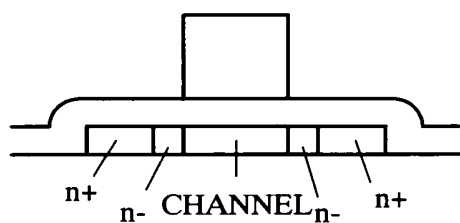


FIG. 34C

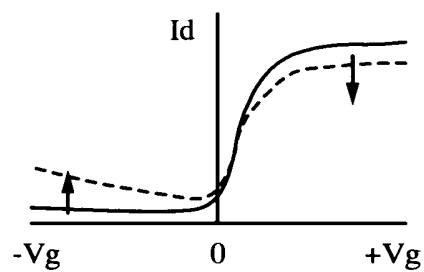


FIG. 34D

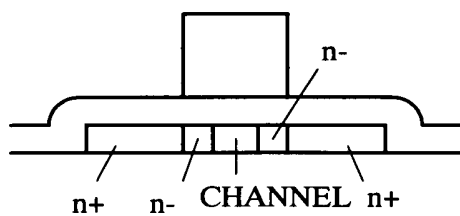


FIG. 34E

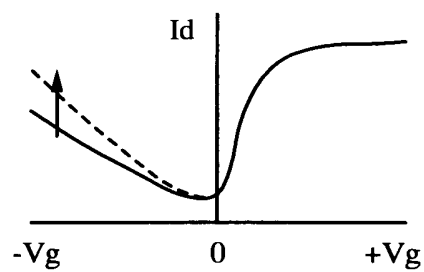


FIG. 34F

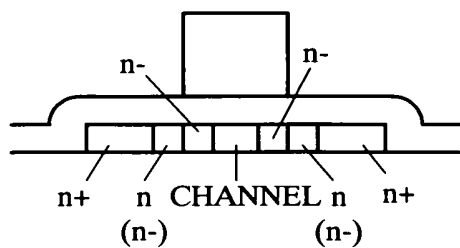


FIG. 34G

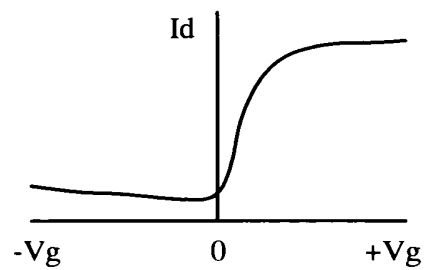


FIG. 34H

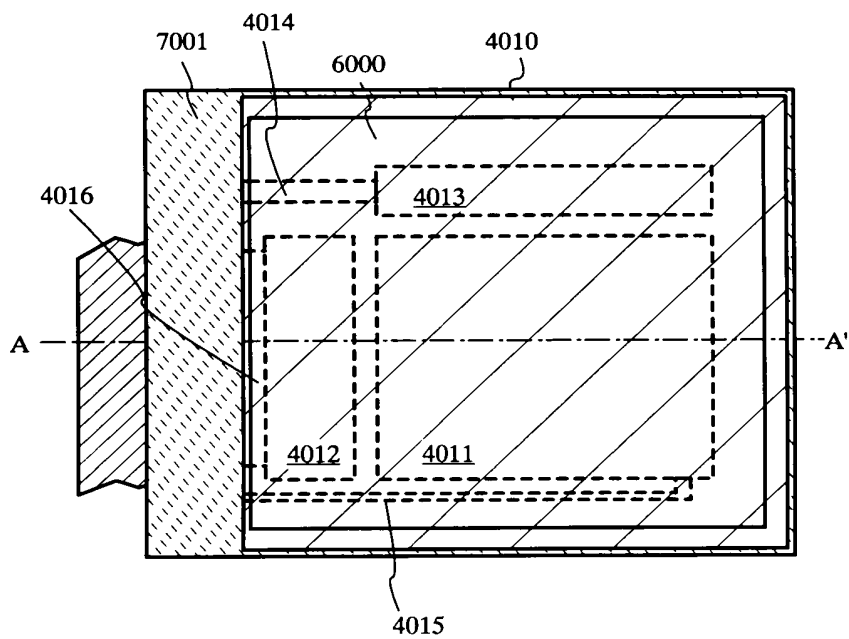


FIG. 35A

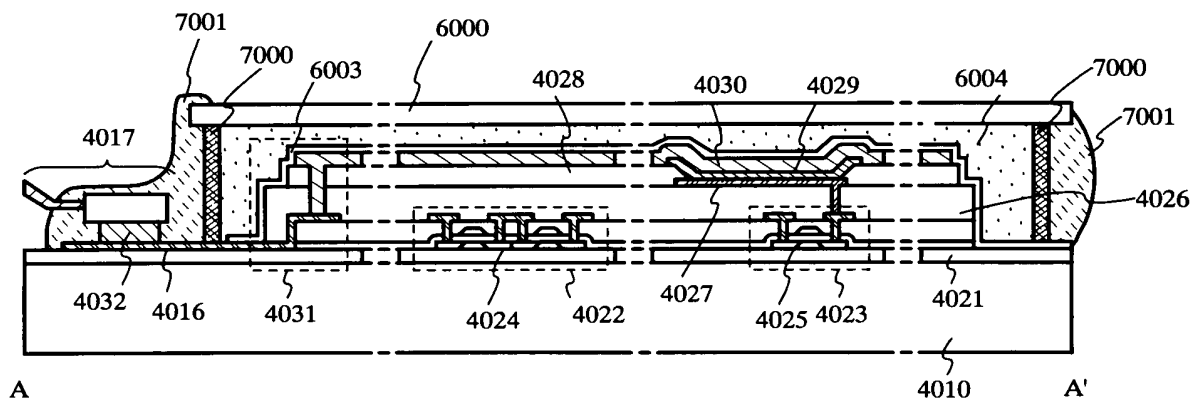


FIG. 35B

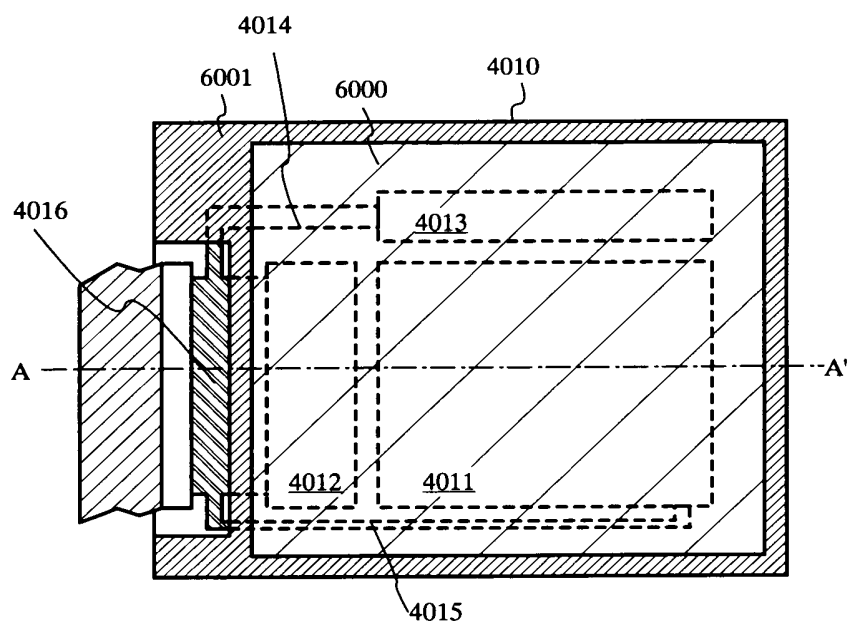


FIG. 36A

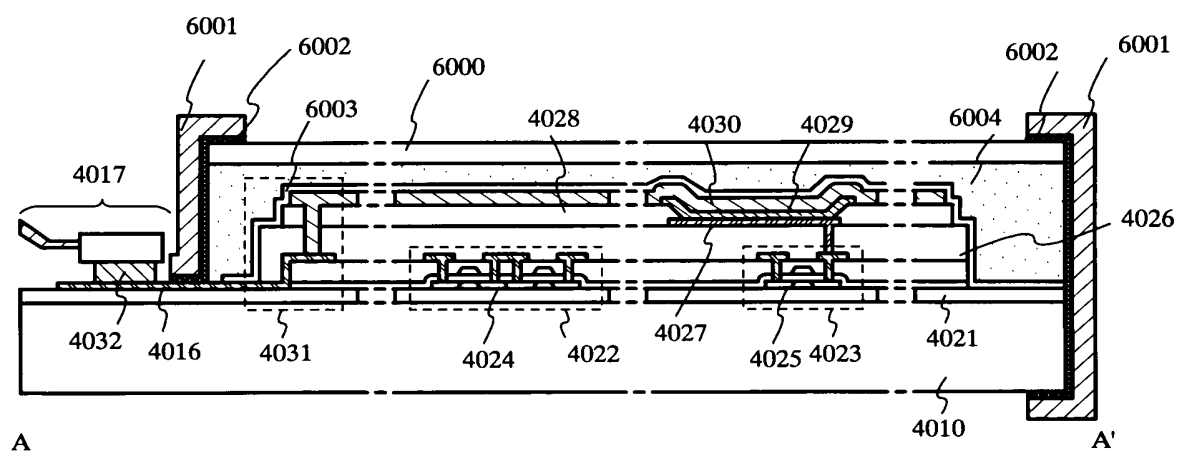


FIG. 36B

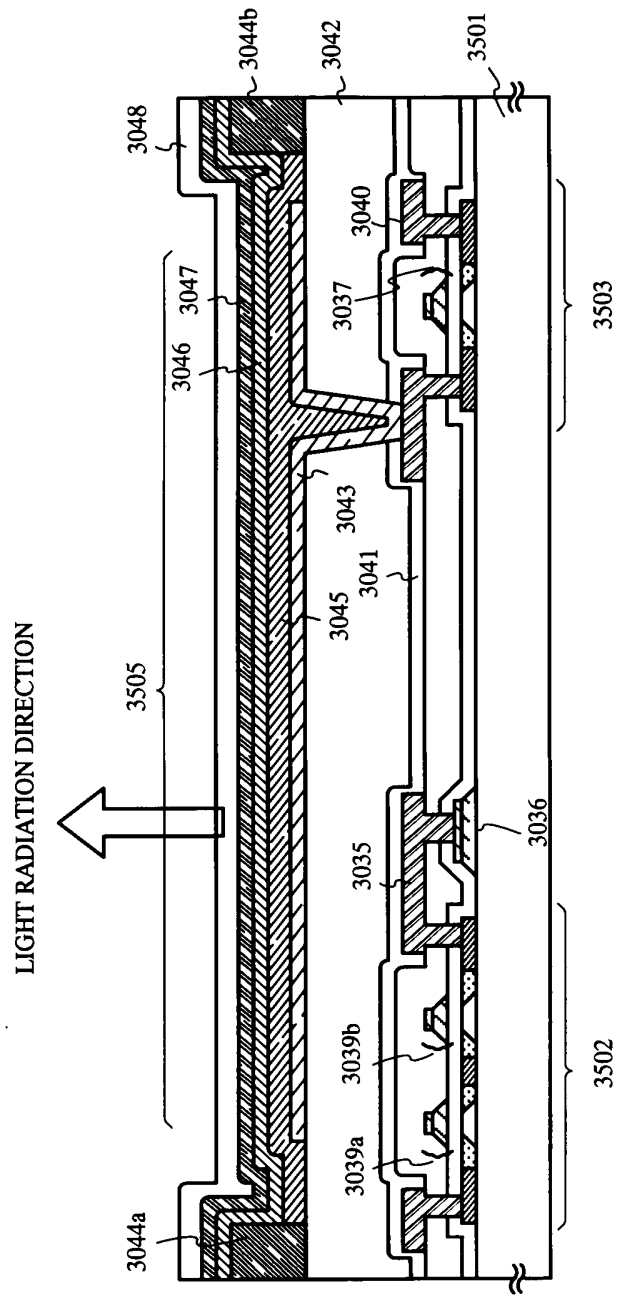


FIG. 37

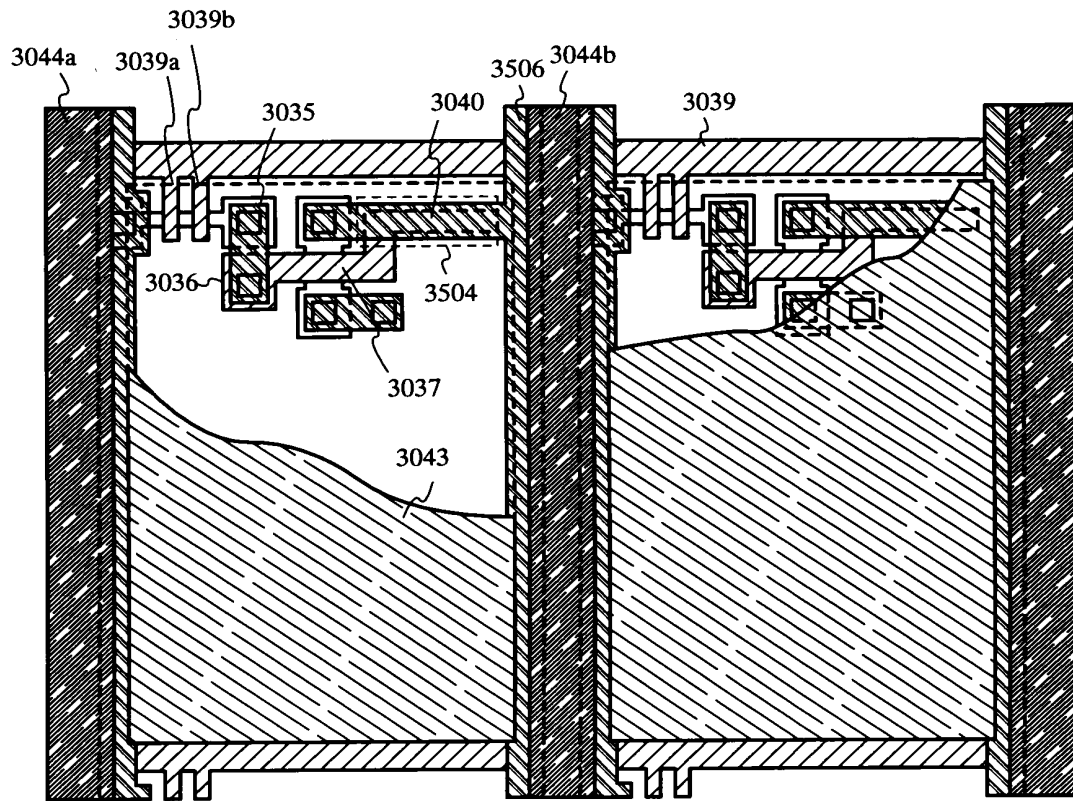


FIG. 38A

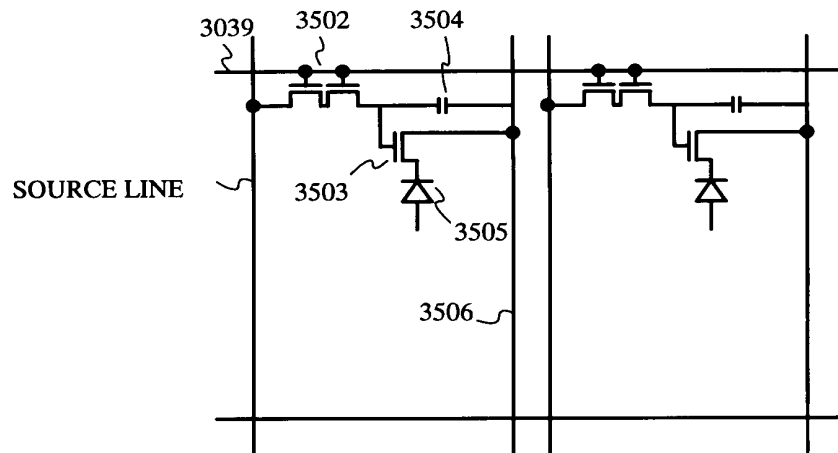


FIG. 38B

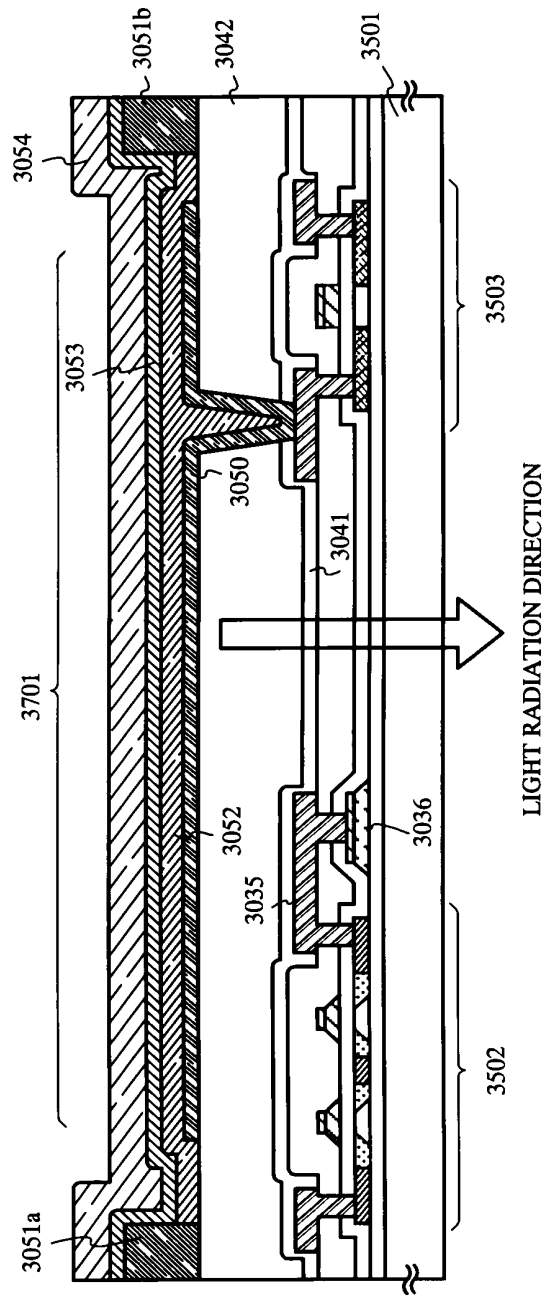


FIG. 39

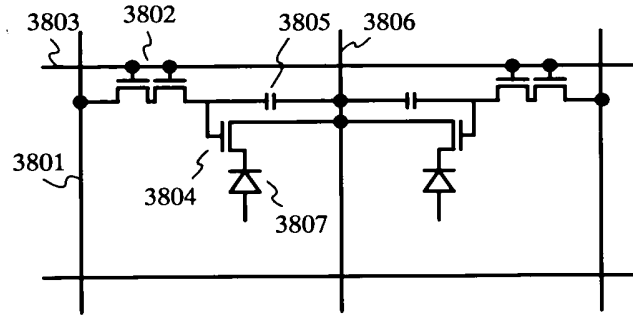


FIG. 40A

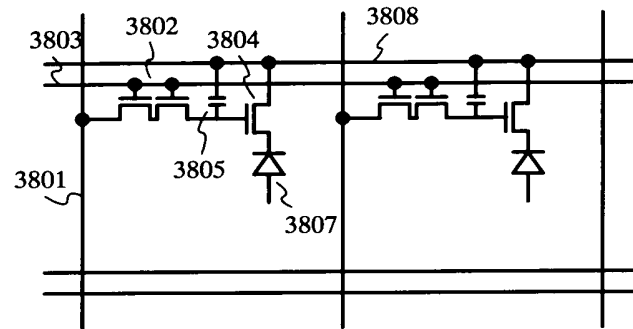


FIG. 40B

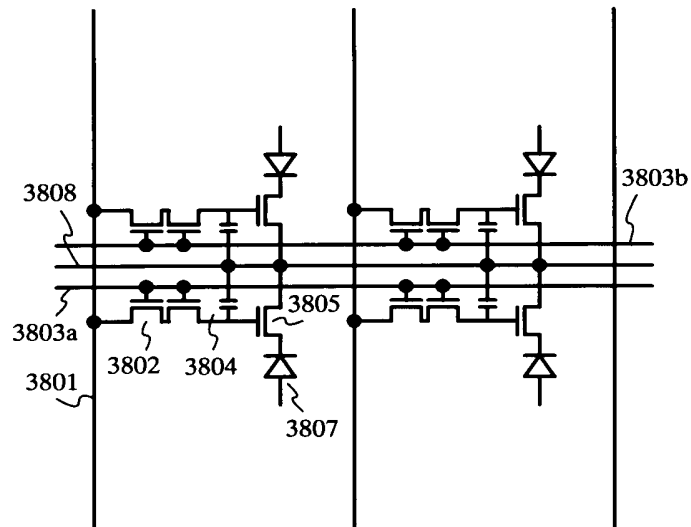


FIG. 40C